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Bt865/865A

Macrovision Process

Rockwell Semiconductor Systems

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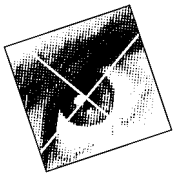

BT865/865A SUPPLEMENT

Purpose

This document serves to define the programming bit map detailing control of the Macrovision anticopy process. The information contained herein is the sole property of Macrovision. For a detailed description of the process, please refer to the Macrovision document. The Bt865 complies with revision 6.1 of the Macrovision specification, and the Bt865A complies with revisions 6, and lower.

Overview

The Macrovision document describes the macrovision process and defines the mapping of bits in order to control the process. This bit mapping is referred to as the Copy Protection Control (CPC) numbers and the Copy Protection Setup (CPS) numbers. The Bt865 directly maps these 4-bit CPC and CPS numbers into 15 8-bit registers and the Bt865A into 18 8-bit registers. This document describes that mapping and briefly describes the function performed. Refer to the Macrovision document for a more detailed description.

Automatic AGC Pulsing

According to the Macrovision specification, the level and timing of the AGC pulses vary according to a precise dynamic pattern. This pattern may be controlled automatically in the Bt865 and Bt865A.

For NTSC, the cycle has a period of about twenty seconds. The pulses are high, at maximum amplitude of 117 IRE above blanking level, for a period of 12 seconds, decay in 16 steps down to blanking level, remain at blanking for 2 seconds, then rise in 16 steps back to maximum level. The AGC pulses are inserted prior to luminance-upsampling in order to filter the 16-step ramp of the 117 IRE. The cycle repeats continuously. The timing of the AGC pulses is based on the field counter, which increments once for each falling edge of VSYNC*. The AGC pulse timing is independent of the sampling rate. AGC pulses have a pulse width of 3.0 µs (+0.2 µs/–0.1µs) for all NTSC modes.

For PAL, the cycle has a period of about thirty seconds. The pulses are high, at maximum amplitude of 810 mV above blanking level, for a period of 12 seconds, and then decay, in 16 steps over a period of 2.6 seconds, toward the blanking level. When the pulse level reaches the point at 100 mV above blanking, pulsation state B commences. State B maintains the pulses at 100 mV, as shown in Table 1.

Table 1. Pulse Amplitudes for States A and B

Line Number	State A	State B
9–13, 321–325	450 mV	100 mV
14–18, 326–330	0 mV	100 mV

Pulsation state B continues for 1.12 seconds. Pulsation state A begins immediately following the next group of lines containing AGC pulses. The change from one state to the other continues to occur every 1.12 seconds. The pulsation mode continues for 12 seconds. After 10 pulsation states, state B begins again, and then the pulse level begins its 16-step rise to the full amplitude of 810 mV above blanking. The pulses remain at full amplitude again for 12 seconds as the cycle repeats continuously. The AGC pulses are inserted prior to luminance-upsampling in order to filter the 16-step ramp of the 117 IRE. The timing of the AGC pulses is based on the field counter, which increments once for each falling edge of VSYNC*. The AGC pulse timing is independent of the sampling rate. AGC pulses have a pulse width of 2.7 µs (+0.2 µs/–0.1µs) for all NTSC modes.

Anticopy Process

This device incorporates an anticopy process technology that is protected by United States patents and other intellectual property rights. The anticopy process is licensed for non-commercial home use only. Reverse engineering or disassembly is prohibited.

The Bt865 anticopy process is implemented according to the revision 6.1 specification by Macrovision, and the Bt865A supports revision 7. All luminance, chrominance, and composite video waveforms include the Macrovision anticopy process. Revision 7 also includes the anticopy process on RGB waveforms.

Closed Captioning

To avoid interfering with the NTSC closed-captioning signal, it is important to ensure that the process is not programmed to occur on lines 21 and 284.

Register Initialization

All registers are write-only and are set to zero following a software reset.

Macrovision Registers

In compliance with attachment 3 of the Macrovision Specification (revision 6.1 for the Bt865; revision 7 for the Bt865A), the following parameters can be varied: pseudo-sync pulse duration, position of first pseudo-sync pulse, pseudo-sync pulse spacing, line numbers containing pseudo-sync/AGC pulse pairs, individual pulse pair enables, line numbers containing the color stripe process, and the amplitude of sync pulses, pseudo-sync pulses, AGC pulses, and back porch pulses.

NOTE: The cycling of AGC pulse levels may be handled automatically by Bt865/Bt865A.

For security purposes, an 8-bit ID register can be read from the device, as described in the Bt864/865, or Bt864A/865A data sheet. The system using the Bt865 or Bt865A should shut off if the correct ID value is not received.

Register mapping into the CPS and CPC numbers is shown in Table 2.

Table 2. Register Mapping

I^2C Address		Register Names	
8-Bit	**7-Bit**	**Bt865**	**Bt865A**(4)
0xD8	0x6C	CPC0, CPC1	CPC0, CPC1
0xDA	0x6D	CPS25, CPS26	CPS25, CPS26
0xDC	0x6E	CPS23, CPS24	CPS23, CPS24
0xDE	0x6F	CPS21, CPS22	CPS21, CPS22
0xE0	0x70	CPS19, CPS20	CPS19, CPS20
0xE2	0x71	CPS17, CPS18	CPS17, CPS18
0xE4	0x72	CPS15, CPS16	CPS15, CPS16
0xE6	0x73	CPS13, CPS14	CPS13, CPS14
0xE8	0x74	CPS11, CPS12	CPS11, CPS12
0xEA	0x75	CPS9, CPS10	CPS9, CPS10
0xEC	0x76	CPS7, CPS8	CPS7, CPS8
0xEE	0x77	CPS5, CPS6	CPS5, CPS6
0xF0	0x78	CPS3, CPS4	CPS3, CPS4
0xF2	0x79	CPS1, CPS2	CPS1, CPS2
0xF4	0x7A	PAD0, CPS0 (1)	PAD0, CPS0 (1)
0xF6	0x7B	(2)	CPS31, CPS32 (3)
0xF8	0x7C		CPS29, CPS30
0xFA	0x7D		CPS27, CPS28

Notes: (1). The upper four bits of this register is a pad of zero's.
(2). Registers 0xF6, 0xF8, 0xFA are not present in the Bt865.
(3). The Bt865A has an address loop built into it to aid in inserting the macrovision CPS numbers in order when using the auto sub-address incrementing feature of the I^2C standard. Start with register 0xF6, after register 0xFA is written the internal address register will now point to register 0xDA. Finish loading the registers, stopping with register 0xF4. Then start another I^2C transaction and load the control register (0xD8) with the appropriate data.
(4). The Bt865A has an additional control bit that will switch the Macrovision functionality from revision 7 to revision 6.1. The location of this control bit is bit D4 in register 0xBC (8-bit address or 0x5E for 7-bit address.) Setting this bit low will result in revision 7 functionality (this is the default value given by the Bt865A datasheet). Setting this bit high will give revision 6.1 functionality and, in this mode, registers 0xF6 to 0xFA are ignored. **If using this mode, load registers according to Table 3.**

Registers

0xD8 (0x6C)

7	6	5	4	3	2	1	0
CPC0[3]	CPC0[2]	CPC0[1]	CPC0[0]	CPC1[3]	CPC1[2]	CPC1[1]	CPC1[0]

0xDA (0x6D)

7	6	5	4	3	2	1	0
CPS25[3]	CPS25[2]	CPS25[1]	CPS25[0]	CPS26[3]	CPS26[2]	CPS26[1]	CPS26[0]

0xDC (0x6E)

7	6	5	4	3	2	1	0
CPS23[3]	CPS23[2]	CPS23[1]	CPS23[0]	CPS24[3]	CPS24[2]	CPS24[1]	CPS24[0]

0xDE (0x6F)

7	6	5	4	3	2	1	0
CPS21[3]	CPS21[2]	CPS21[1]	CPS21[0]	CPS22[3]	CPS22[2]	CPS22[1]	CPS22[0]

0xE0 (0x70)

7	6	5	4	3	2	1	0
CPS19[3]	CPS19[2]	CPS19[1]	CPS19[0]	CPS20[3]	CPS20[2]	CPS20[1]	CPS20[0]

0xE2 (0x71)

7	6	5	4	3	2	1	0
CPS17[3]	CPS17[2]	CPS17[1]	CPS17[0]	CPS18[3]	CPS18[2]	CPS18[1]	CPS18[0]

0xE4 (0x72)

7	6	5	4	3	2	1	0
CPS15[3]	CPS15[2]	CPS15[1]	CPS15[0]	CPS16[3]	CPS16[2]	CPS16[1]	CPS16[0]

0xE6 (0x73)

7	6	5	4	3	2	1	0
CPS13[3]	CPS13[2]	CPS13[1]	CPS13[0]	CPS14[3]	CPS14[2]	CPS14[1]	CPS14[0]

0xE8 (0x74)

7	6	5	4	3	2	1	0
CPS11[3]	CPS11[2]	CPS11[1]	CPS11[0]	CPS12[3]	CPS12[2]	CPS12[1]	CPS12[0]

0xEA (0x75)

7	6	5	4	3	2	1	0
CPS9[3]	CPS9[2]	CPS9[1]	CPS9[0]	CPS10[3]	CPS10[2]	CPS10[1]	CPS10[0]

0xEC (0x76)

7	6	5	4	3	2	1	0
CPS7[3]	CPS7[2]	CPS7[1]	CPS7[0]	CPS8[3]	CPS8[2]	CPS8[1]	CPS8[0]

0xEE (0x77)

7	6	5	4	3	2	1	0
CPS5[3]	CPS5[2]	CPS5[1]	CPS5[0]	CPS6[3]	CPS6[2]	CPS6[1]	CPS6[0]

0xF0 (0x78)

7	6	5	4	3	2	1	0
CPS3[3]	CPS3[2]	CPS3[1]	CPS3[0]	CPS4[3]	CPS4[2]	CPS841]	CPS4[0]

0xF2 (0x79)

7	6	5	4	3	2	1	0
CPS1[3]	CPS1[2]	CPS1[1]	CPS1[0]	CPS2[3]	CPS2[2]	CPS2[1]	CPS2[0]

0xF4 (0x7A)

7	6	5	4	3	2	1	0
RES	RES	RES	RES	CPS0[3]	CPS0[2]	CPS0[1]	CPS0[0]

0xF6 (0x7B)

7	6	5	4	3	2	1	0
CPS31[3]	CPS31[2]	CPS31[1]	CPS31[0]	CPS32[3]	CPS32[2]	CPS32[1]	CPS32[0]

0xF8 (0x7C)

7	6	5	4	3	2	1	0
CPS29[3]	CPS29[2]	CPS29[1]	CPS29[0]	CPS30[3]	CPS30[2]	CPS30[1]	CPS30[0]

0xFA (0x7D)

7	6	5	4	3	2	1	0
CPS27[3]	CPS27[2]	CPS27[1]	CPS27[0]	CPS28[3]	CPS28[2]	CPS28[1]	CPS28[0]

Register Settings

Table 3. Bt865 Macrovision Default Values

Register Value		NTSC		PAL	
8-bit	**7-bit**	**24.55 MHz**	**27.00 MHz**	**27.00 MHz**	**29.50 MHz**
0xD8	0x6C	0x3E	0x3E	0x3E	0x3E
0xDA	0x6D	0x60	0x60	0xE0	0xE0
0xDC	0x6E	0x0F	0x0F	0x3F	0x3F
0xDE	0x6F	0x0F	0x0F	0x3F	0x3F
0xE0	0x70	0x00	0x00	0x00	0x00
0xE2	0x71	0x00	0x00	0x00	0x00
0xE4	0x72	0xF0	0xF0	0xFE	0xFE
0xE6	0x73	0x4F	0xCF	0xC7	0x07
0xE8	0x74	0x92	0x26	0xB6	0xD9
0xEA	0x75	0x48	0x6D	0x91	0xB6
0xEC	0x76	0x92	0x92	0x8E	0x8E
0xEE	0x77	0x9D	0x9D	0xA0	0xA0
0xF0	0x78	0x88	0x88	0x17	0x17
0xF2	0x79	0x12	0x12	0xF4	0xF4
0xF4	0x7A	0x01	0x01	0x02	0x02

Table 4. Bt865A Macrovision Default Values

Register Value		NTSC		PAL	
8-bit	**7-bit**	**24.55 MHz**	**27.00 MHz**	**27.00 MHz**	**29.50 MHz**
0xD8	0x6C	0x3E	0x3E	0x3E	0x3E
0xDA	0x6D	0x60	0x60	0x60	0x60
0xDC	0x6E	0x0F	0x0F	0x3F	0x3F
0xDE	0x6F	0x0F	0x0F	0x3F	0x3F
0xE0	0x70	0x00	0x00	0x00	0x00
0xE2	0x71	0x00	0x00	0x00	0x00
0xE4	0x72	0xF0	0xF0	0xFE	0xFE
0xE6	0x73	0xCF	0x0F	0xC7	0x47
0xE8	0x74	0x96	0xB9	0xB6	0x4B
0xEA	0x75	0x48	0x6D	0x91	0xB6
0xEC	0x76	0xB6	0xB6	0xA8*(1)*	0xA8*(1)*
0xEE	0x77	0xD5	0xD5	0x62	0x62
0xF0	0x78	0xB0	0xB0	0x55	0x55
0xF2	0x79	0x72	0x72	0xA4	0xA4
0xF4	0x7A	0x0D	0x0D	0x05	0x05
0xF6	0x7B	0xFF	0xFF	0x55	0x55
0xF8	0x7C	0x2C	0x2C	0x27	0x27
0xFA	0x7D	0xC8	0xD0	0x40	0x48

Notes: (1). For the 3 line color stripe version for PAL, change this value to OxA9.

Table 5. Bt865A Macrovision Registers values for NTSC 2-Line version with 17 line spacing

Bt865A Registers		
I²C Address		Reg. values
8bit	7bit	
0xEC	0x76	0x3C
0xEE	0x77	0xD1
0xFO	0x78	0x32
0xF2	0x79	0xD2
Note: Only registers 0xEC to 0xF2 inclusive are different from the default values given in Table 4. These values are valid for both 24.55 Mhz and 27 Mhz.		

Table 6. Bt865A Macrovision Register, Mapping, and Values for PAL-13.5 Mhz, P203 configuration

Bt865A Registers		
I²C Address		Reg. values
8bit	7bit	
0xD8	0x6C	0x36
0xDA	0x6D	0x60
0xDC	0x6E	0x7E
0xDE	0x6F	0xFE
0xEO	0x70	0x54
0xE2	0x71	0x01
0xE4	0x72	0xFF
0xE6	0x73	0x01
0xE8	0x74	0xD5
0xEA	0x75	0x73
Note: Only registers 0xD8 to0xEA, inclusive, are different from the default values given in Table 4.		

Rockwell Semiconductor Systems, Inc.
9868 Scranton Road
San Diego, CA 92121-3707
(619) 452-7580
1(800) 2-BT-APPS
FAX: (619) 452-1249
Internet: apps@brooktree.com
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